AMENDMENTS TO THE CLAIMS

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. **(Currently Amended)** A system for measuring a signal propagation delay, said system being adapted to electrically communicate with at least one transmitter and at least one receiver, said system comprising:

a first bit sequence generator used to generate a first sequence of bits that is to be transmitted through an object with, an unknown propagation delay[[,]];

a second bit sequence generator that receives said first sequence of bits from said object, said second bit sequence generator generating a second sequence of bits identical to said first sequence; and

a controller that receives said first and second sequences of bits, said controller compares said sequences to confirm that said sequences are identical, instructs said first bit sequence generator to inject a predefined bit error into a third sequence of bits while simultaneously starting a clock count from a clock source, maintains said count that is incremented each time said controller checks for said bit error, stops incrementing said count when said bit error is detected, and computes said propagation delay by reference to said count.

2. **(Original)** The system of claim 1, wherein said object is one of a length of fiber optic cable, an electronic device and an opto-electronic device.

3. **(Original)** The system of claim 1, wherein said first BS generator and said second BS generator produce identical output from identical input.

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4. **(Original)** The system of claim 1, wherein said first BS generator and said second BS generator each operate at a frequency of a clock signal generated by said clock source.

5. **(Original)** The system of claim 1, wherein said controller computes an ideal delay value from said first and second bit sequences and uses said ideal delay value to compute said propagation delay.

6. **(Original)** The system of claim 5 wherein said predefined bit error is generated for a particular bit position and said controller uses said particular bit position to calculate said propagation delay.

7. **(Original)** The system of claim 1 wherein said predefined bit error is generated for a particular bit position and said controller uses said particular bit position to calculate said propagation delay.

8. **(Original)** In a system for measuring a signal propagation delay, said system being adapted to electrically communicate with at least one transmitter and at least one receiver, said system comprising a first bit sequence generator, a second bit sequence generator, a clock source and a controller, a method for computing the signal propagation delay comprising the steps of:

computing an ideal delay value;

injecting an error into a bit sequence generated by the bit sequence generators and maintaining a clock count from the clock source until the controller receives said error;

determining a bit position for said error in said bit sequence; and

calculating the propagation delay from said ideal delay value, said clock count and said bit position.

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9. **(Currently Amended)** The method of claim 8 wherein said step of computing an ideal delay value further comprises the steps of:

setting an initial value for said delay;

generating a first sequence of bits;

sending said first sequence of bits to the at least one transmitter, which sends said first sequent of bits to the at least one receiver, which sends said first sequence of bits to a programmable delay device;

delaying said first sequence of bits received from the at least one receiver;

generating a second sequence of bits, said second sequence of bits also being sent to the at least one transmitter, the at least one receiver and said programmable delay device;

comparing said first sequence of bits to said second sequence of bits to determine if there are any bit errors;

if said bit errors are encountered, incrementing said initial value for said delay and repeating said first and said second ~~generating steps;~~ generating steps; and

if said bit errors are not encountered, computing said ideal delay.

10. **(Original)** The method of claim 9 wherein the steps of generating said first and second sequences of bits includes generating a series of bit groups.

11. **(Original)** The method of claim 10 wherein each of said bit groups contains at least 80 bits.

12. **(Original)** The method of claim 8 wherein said step of using said ideal delay value to gather data includes the steps of:

resetting said clock counter value to zero and beginning a new count;

including a predefined bit error in a next bit group generated;

generating a subsequent bit group;

delaying any additional bits received from said receiver by said ideal delay;

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comparing said subsequent bit group to said additional bits;

if said comparing does not detect said predefined bit error, generating a second subsequent bit group until said comparing step detects said predefined error; and

if said comparing detects said predefined bit error, storing said clock counter value and computing said propagation delay.

13. **(Original)** The method of claim 8, wherein said object is one of a length of fiber optic cable, an electronic devicc and an opto-electronic device.

14. **(Original)** In a computerized system comprising a circuit board having electrical circuitry connecting a first bit sequence (BS) generator, a serializer/deserializer (SERDES), a programmable delay, a deserializer, a second BS generator, a controller, and a clock source, said system further comprising an transmitter and a receiver electrically connected to the circuit board, a method for computing a signal propagation delay through an object comprising the steps of:

initializing the first bit sequence (BS) generator, the serializer/ deserializer (SERDES), the programmable delay, the deserializer, the second BS generator, the controller, the clock source, the circuit board, the transmitter and the receiver;

aligning data from the receiver with a clock signal from the clock source and storing a clock counter value;

identifying an ideal delay value for the programmable delay;

using said ideal delay value to gather data needed to determine the propagation delay; and

calculating the propagation delay using said data.

15. **(Currently Amended)** The method of claim 14 wherein said step of identifying an ideal delay further comprises the steps of:

setting an initial value for the delay;

generating a first sequence of bits;

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sending said first sequence of bits to the transmitter, which sends said first sequent of bits to the receiver, which sends said first sequence of bits to the programmable delay;

delaying said first sequence of bits received from the receiver;

generating a second sequence of bits, said second sequence of bits also being sent to the transmitter, the receiver and the programmable delay;

comparing said first sequence of bits to said second sequence of bits to determine if there are any bit errors;

if said bit errors are encountered, incrementing said initial value for said delay and repeating said first and said second ~~generating steps;~~ <u>generating steps; and</u>

if said bit errors are not encountered, computing said ideal delay.

16. **(Original)** The method of claim 15 wherein the steps of generating said first and second sequences of bits includes generating a series of bit groups.

17. **(Original)** The method of claim 16 wherein each of said bit groups contains at least 80 bits.

18. **(Original)** The method of claim 17 wherein said step of using said ideal delay value to gather data includes the steps of:

resetting said clock counter value to zero and beginning a new count;

including a predefined bit error in a next bit group generated;

generating a subsequent bit group;

delaying any additional bits received from the receiver by said ideal delay;

comparing said subsequent bit group to said additional bits;

if said comparing step does not detect said predefined bit error, generating a second subsequent bit group until said comparing step detects said predefined error; and

if said comparing step detects said predefined bit error, storing said clock counter value and computing said propagation delay.

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19. **(Original)** The method of claim 18, wherein said predefined bit error is generated for a particular bit position and said controller uses said particular bit position to calculate said propagation delay.

20. **(Original)** The method of claim 14, wherein said object is one of a length of fiber optic cable, an electronic device and an opto-electronic device.

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